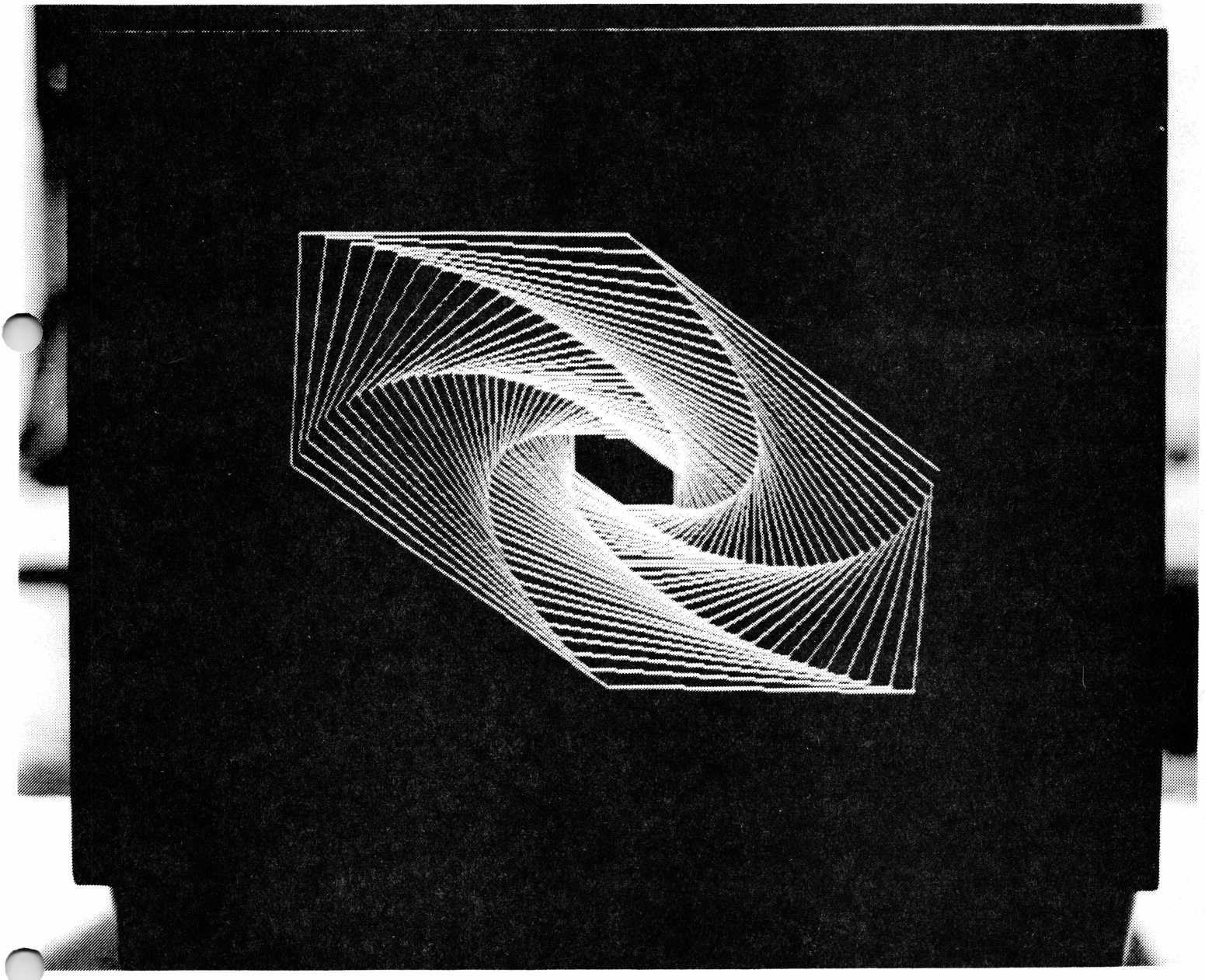
MICRO TECHNOLOGY UNLIMITED

Introduces its revolutionary

V i s a b l e M e m o r y

to the KIM-1 user

A low-cost high resolution graphic display device
designed specifically for the KIM-1 by
Hal Chamberlin



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KIM - 1 8K MEMORY / RASTER GRAPHIC DISPLAY GENERATOR

The MTU Visable Memory is a unique concept in microcomputer memory systems. For about what you would expect to pay for either an 8K memory board or a dense dot raster graphic display board alone you can have both! The MTU Visable Memory is an 8K memory add-on to the Commadore KIM-1 system which includes the circuitry to simultaneously display the memory contents as 64,000 dots on a TV monitor. Unlike many other add-on memory boards, this one is designed for the KIM-1 and is merely connected in parallel with the expansion connector on the KIM-1 with two wires also connecting to the application connector. No modifications to the KIM-1 itself are necessary. The KIM-1 continues to run at full speed with no wait states and no software overhead or CPU time required to refresh the display. Also there is no snow or other visable interference on the screen when the display memory is being accessed or changed by the KIM CPU.

Applications of the Visable Memory are endless. The basic display format is 200 lines of 320 dots per line. With the optional character display package, up to 18 lines of 40 upper and lower case characters with true descenders can be displayed. As many as 53 characters per line is possible with some sacrifice in character generation speed. With alternate font tables (5X9 is included in the optional software package), characters of varying size and shape can be displayed simultaneously as well as real subscripts, superscripts, and proportional spacing. In short, the Visable Memory makes an exceptionally versatile text display. With the graphing routines in the software package, many kinds of graphs and charts can be displayed. With the "BASIC Patch Package", soon to be available, KIM BASIC can make full use of the display for both text and graphics applications.

Animated and interactive graphics capabilities make all kinds of games possible with a degree of realism never before available on a hobby computer. Since there is no snow or other interference on the screen ever, programming of moving images is completely unrestricted.

Extensive use of low power Shottky IC's and 4K dynamic RAM's is responsible for the low power consumption, low cost, and small size of the board. Problems experienced with dynamic memory in some other systems are absent in this board due to the superior bus control achitecture of the KIM-1 and advanced circuit design. The circuitry that generates the display also refreshes the memory automatically as it scans.

Jumpers or an optional DIP switch select the 8K block of addresses to be assigned to the board. An optional jumper selectively disables the top or bottom half of the display thus allowing 4K to be used for program storage without showing up as random patterns on the screen. The "Decode Enable" and "Vector Fetch" signals needed when The KIM is expanded beyond 4K are generated by the board and need simply be connected to the proper pins of the application connector. Up to three Visable Memory boards may be connected to the KIM without overloading the bus.

The board is designed to be mounted benieth the KIM-1. It is the same width as the KIM and the 44 pin edge connector is in the same position as the KIM's expansion connector.

SPECIFICATIONS

Display Format: 200 lines, 320 dots per line, non-interlace
Scanning Frequencies: (derived from KIM-1 crystal clock)
Horizontal: 15,625 Hz, Vertical: 60.1 Hz.
Required video bandwidth: 4 mHz minimum
Output: 1.25 V p-p composite video into 75 ohms, sync negative
Adjustments: One, dot sync (factory aligned on assembled units)
Power requirements: +7.5 volts unregulated .25 amp, +16 volts unregulated .25 amp.
Sockets: 16 memory IC's, address and blanking jumpers, and vector fetch gate (7430) are socketed.
Memory type: 22 pin 4K dynamic RAM, National Semi. MM5280 or equ.
Access time: greater than 100NS data stable time prior to fall of $\overline{\text{Phase 2}}$ clock
Cycle time: internally synchronized to 1.0mHz $\overline{\text{Phase 2}}$ clock from host system
Printed circuit board: 11" wide by 5" tall exclusive of gold-plated edge connector, plated-through holes
Inclusions: bare or assembled and tested board; instruction manual containing schematic, trouble-shooting tips, and memory diagnostic (fun to watch!)
Price: Assembled and tested - $289.00
Bare board - $40.00
Kits are not available.
Quantity discounts are available, please request on letterhead a current MTU price list.
Delivery: First retail delivery is January, 1978. Standard delivery schedule is stock to 2 weeks for retail orders. Delivery on larger quantities is individually negotiated.

PIN CONNECTIONS

Signal	KIM	K-1008	Signal	KIM	K-1008
SYNC	E-1	N.C.	ADDR BUS 0	E-A	A
RDY	E-2	N.C.	ADDR BUS 1	E-B	B
PHASE 1	E-3	N.C.	ADDR BUS 2	E-C	C
IRQ	E-4	N.C.	ADDR BUS 3	E-D	D
SET OVERFLOW	E-5	N.C.	ADDR BUS 4	E-E	E
NON-MASK INT.	E-6	N.C.	ADDR BUS 5	E-F	F
RESET	E-7	N.C.	ADDR BUS 6	E-H	H
DATA BUS 7	E-8	8	ADDR BUS 7	E-J	J
DATA BUS 6	E-9	9	ADDR BUS 8	E-K	K
DATA BUS 5	E-10	10	ADDR BUS 9	E-L	L
DATA BUS 4	E-11	11	ADDR BUS 10	E-M	M
DATA BUS 3	E-12	12	ADDR BUS 11	E-N	N
DATA BUS 2	E-13	13	ADDR BUS 12	E-P	P
DATA BUS 1	E-14	14	ADDR BUS 13	E-R	R
DATA BUS 0	E-15	15	ADDR BUS 14	E-S	S
K6	E-16	N.C.	ADDR BUS 15	E-T	T
SING. STP. OUT	E-17	N.C.	PHASE 2	E-U	N.C.
+7.5 UNREG	N.C.	18	$\overline{\text{READ/WRITE}}$	E-V	V
VECTOR FETCH	A-J	19	READ/WRITE	E-W	W
DECODE ENAB.	A-K	20	*+16 UNREG*	***	X
+5 REG.	E-21	N.C.	$\overline{\text{PHASE 2}}$	E-Y	Y
GROUND	E-22	22	RAM R/W	E-Z	N.C.

*** This signal must connect to the K-1008 only, not the KIM!

INTERFACING

The K-1008 Visable Memory is designed for the simplest possible interfacing to the KIM-1 microcomputer. Simply wire the K-1008 in parallel (except for pin X which is the PLL TEST pin) with the Expansion connector on the KIM-1 itself. Since the K-1008 edge connector is in the same relative position as the expansion connector, two 44 pin standard edge connectors wired together may be used. If additional expansion is not anticipated, it is possible to merely solder wires to the edge fingers on the boards. When wiring several edge connectors together for a large system, it is desirable that the pin 22 wiring (Ground) be done with braid (solder wick works well) or several strands of hookup wire. MTU will shortly have a simple, inexpensive 5 slot motherboard available that allows additional KIM compatible boards to be stacked undernieth and parallel to the KIM board.

The VECTOR FETCH and DECODE ENABLE signals provided by the K-1008 must also be connected to the appropriate inputs on the application connector to satisfy the KIM requirements when memory beyond 4K is added (see the pin connection table).

Up to 3 K-1008 boards can be connected to the KIM without buffering. However the 74LS30 that generates the VECTOR FETCH signal should be removed from all but one of the boards to minimize address bus loading.

The video output is designed with a precise 75 ohm source impedance to simplify connection to a standard monitor even over long lengths of coax cable. If only one monitor is at the end of the cable, termination at the monitor is not required since the K-1008 will absorb all line reflections. If several monitors are daisy-chained, the one at the far end must be terminated in 75 ohms to prevent the reflections from showing up on the middle monitors.

Connection to computers other than the KIM-1 is possible but the system must utilize either a Motorola 6800 or one of the MOS technology CPU's (such as a 6502, 6512, etc.) and must have a 1.0mHz clock. This includes OSI 6502 based products, SWTP 6800 products, APPLE, ECD, and Commodore but not the Altair 680 since it runs at .5mHz. Also, none of the 8080 or Z-80 based systems can be used since their bus control cannot support the flip-flop access method mentioned earlier. The extra KIM-related circuitry may be left intact when connecting to other systems. The K-1008 can be used with a "Kimsi" motherboard but connections between the K-1008 and the KIM should still be done at the KIM's expansion connector and not the Kimsi edge connectors.

Address jumpering on the board can be set at any 8K boundary. It is recommended that the first K-1008 be jumpered for 2000-3FFF, the second for 4000-5FFF, etc. Although physically possible, it is not recommended that the board be jumpered for either 0000 or E000 since it will then interfere with memory already on the KIM.

It is not possible to de-populate the board to 4K because all even addresses access one group of 8 RAM chips and all odd addresses access the other group. This was done to conserve power while allowing for self-refresh by the video generator.

The board may be run on +12 and +5 volt regulated power supplies by simply shorting the two outside pins of each on-board regulator IC together.

Programming of the K-1008 to display text and graphics is very straightforward. The display is essentially a matrix of dots with 200 rows of 320 dots per row. For addressing purposes the dots can be numbered from 0 to 63,999 with dot 0 being the upper left-hand corner dot, dot 319 being at the upper right corner, dot 320 being the leftmost dot on the next row down, and 63,999 being the lower right-hand corner dot. Eight horizontally adjecant dots make up one byte of memory with the position of the dots on the display corresponding to the position of the bits in the byte. Thus dot 0 is the leftmost bit (bit 7) of the first byte in the visable memory (generally at memory address 2000_{16}). Conversely dot 319 would be the rightmost bit (bit 0) of the fourtieth byte (typically address 2037_{16}).

Usually graphics programming is performed using the X-Y method of identifying a particular dot position. Although the origin of the coordinate system can be assumed to be anywhere, it is convenient to place it at the lower left corner of the display. Thus all of the displayable points are in the first quadrant and X and Y are always positive numbers. To convert from X-Y point coordinates to a dot number is a simple matter involving evaluation of the equation: DOT # = (199-Y)*320+X . Conversion from the dot number to a byte address and bit number (assuming most significant bit is bit 0) is as follows: BYTE ADDR = VM BASE ADDR + INT(BIT #/8); BIT # = REM(BIT #/8) . Going directly from coordinates to byte address and bit number is as follows: BYTE ADDR = VM BASE ADDR + (199-Y)*40+INT(X/8); BIT # = REM(X/8) . Note that the multiplication by 40 can be accomplished in steps as follows: A*40=(A+A*4)*8 where multiplication by 4 and 8 is accomplished by shifting left 2 and 3 positions respectively. Divison by 8 is accomplished by shifting right 3 positions.

Once the byte and bit addresses are found, the dot may be turned on with the logical OR instruction, turned off with an AND instruction, or flipped with an EOR instruction. It is convenient to write subroutines that accept X and Y coordinates as input and set, reset, flip, write, or read a dot. These would in turn call a subroutine to compute the byte and bit addresses from X and Y coordinates. A more sophisticated subroutine would accept the coordinates of the endpoints of a line and fill in the points forming the closest approximation to the straight line between them. Characters may be drawn either as line segments or a dot matrix by using a font table and calls to the appropriate routine. In special cases drawing speed may be greatly increased by handling the 8 dots in a byte simultaneously.

Since the X coordinate may be as large as 319 which requires 9 bits to represent, the X coordinate must be a double-precision number. Although Y will fit into 8 bits, it too should be double precision for consistency and software compatibility with future display hardware upgrades. It is entirely possible that within two years from now we will see the introduction of a 640 wide by 400 high display using 16K dynamic RAM's!

Although it is a lot of fun to build up graphic subroutines yourself, it is possible that some users would prefer to have the work done for them. A set of utility routines including those discussed above plus some others and a full 320x200 LIFE game are under development and will be available shortly for $20.00 as printed, heavily commented source listings.

ABBREVIATED PRINCIPLES OF OPERATION

The K-1008 Visable Memory is basically an 8K dynamic memory board. However instead of letting the memory refresh cycles go to waste, the data read is formatted into a video signal and sent out. Thus, depending on your point of view, it is either a dynamic board with "visable" refresh or a static video display board.

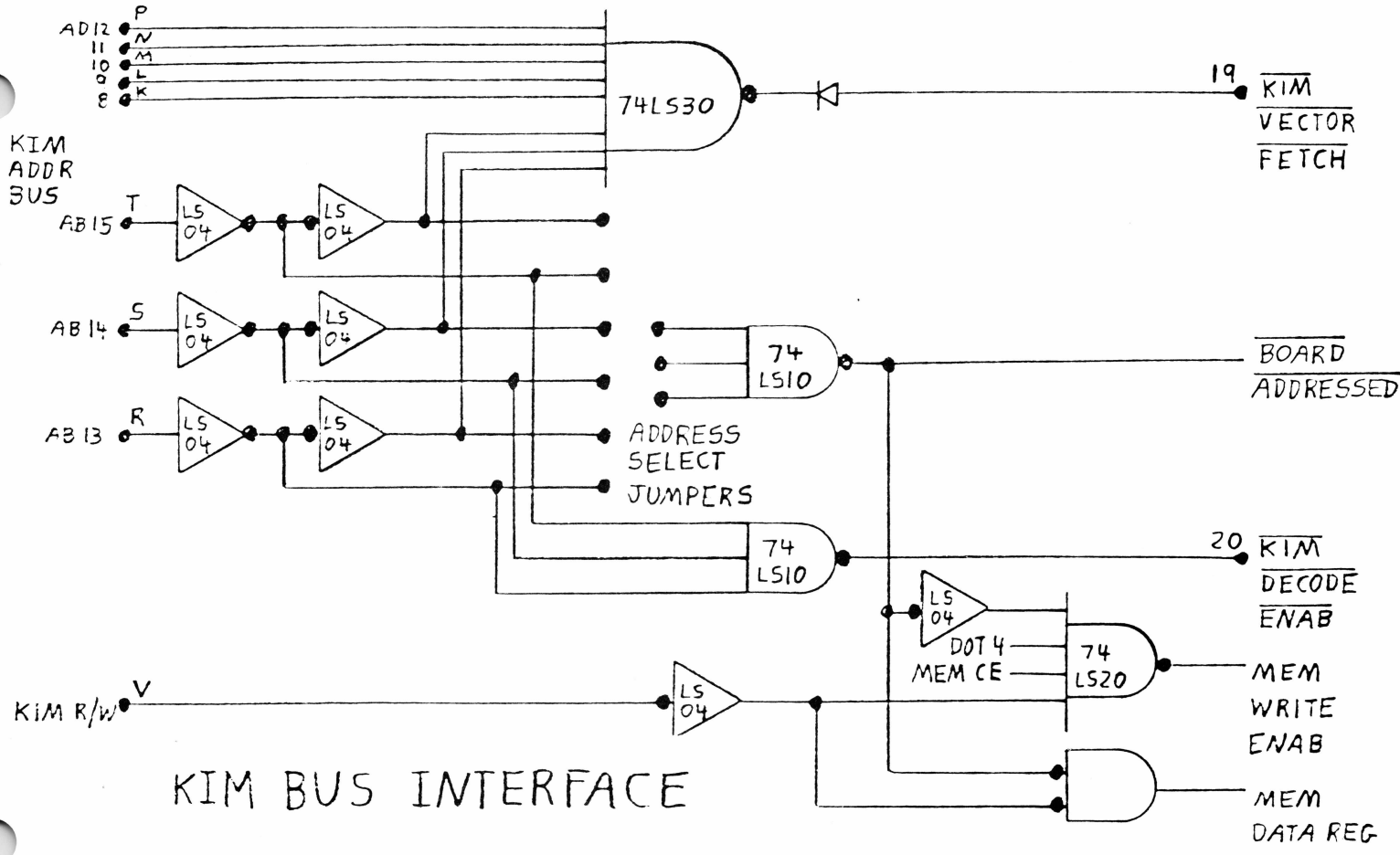
The key to the board's remarkable properties is the 6502 bus itself. A symmetrical 1.0 mHz two-phase clock is used by the KIM-1. The 6502 microprocessor really accesses memory only during Phase 2 with Phase 1 being used for setup. Thus the visable memory can use the 500NS period during Phase 1 to access the memory for display and then turn the memory over to the 6502 during phase 2. Access times approaching 300NS are required with this scheme but that figure is actually rather slow compared with modern 4K dynamic RAM standards. It is this "flip-flop" sharing between microprocessor and display that makes glitchless display quality possible under all operating conditions.

All of the board's timing is derived from an 8mHz oscillator which is phase-locked to the falling edge of the Phase 2 signal from the KIM. Each cycle of this oscillator represents 1 dot on the display. Every 4 cycles represents a single memory cycle which is alternately assigned to the video generator and the KIM as previously described. Timing within each memory cycle is generated by decoding the divide-by-4 counter. Every 8 cycles represents a byte of display data. Forty byte times make up the visable portion of a horizontal line and 24 more are allowed for retrace. Two-hundred horizontal scan cycles make up the visable portion of the vertical scan while 60 more are allowed for retrace. Thus the 1.0mHz KIM clock is multiplied to 8.0mHz and then divided down to 60Hz in several steps.

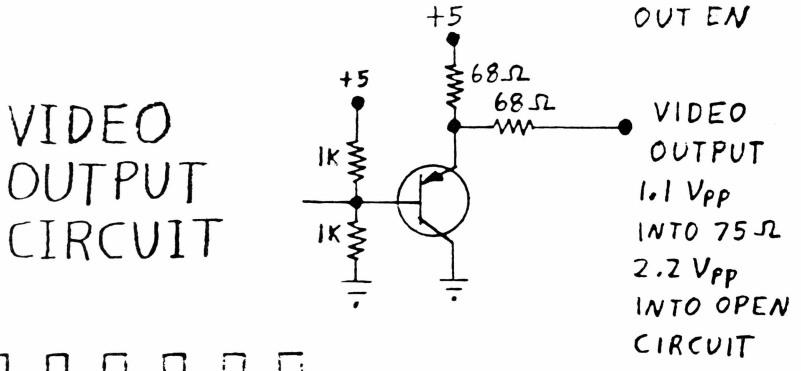
Dynamic RAM's have the desirable property that power is drawn only when they are clocked through a cycle. A power saver circuit determines precisely when each RAM chip is being accessed and only then does it get a clock pulse. Net power consumption from the +16 volt supply to refresh the display alone is less than 100MA. This rises to about 250MA with 100% access by the KIM. However, in the case of multiple boards, the KIM can only access one at a time so in effect the first board may require as much as 250MA but each additional one needs only 100MA! Exclusive use of low power Schottky for the peripheral logic keeps +5 volt current consumption under 250MA per board. As a result, the simple K-1000 power supply is rated to drive the KIM and 2 visable memory boards and typically can power 3 of them.

Negative 5 volts for the RAM's substrate bias is derived from a charge-pump cirucit powered from the +12 volt internal supply. On board regulators for both +5 and +12 allow the use of unregulated power supplies or the "raw" outputs of the K-1000 power supply.

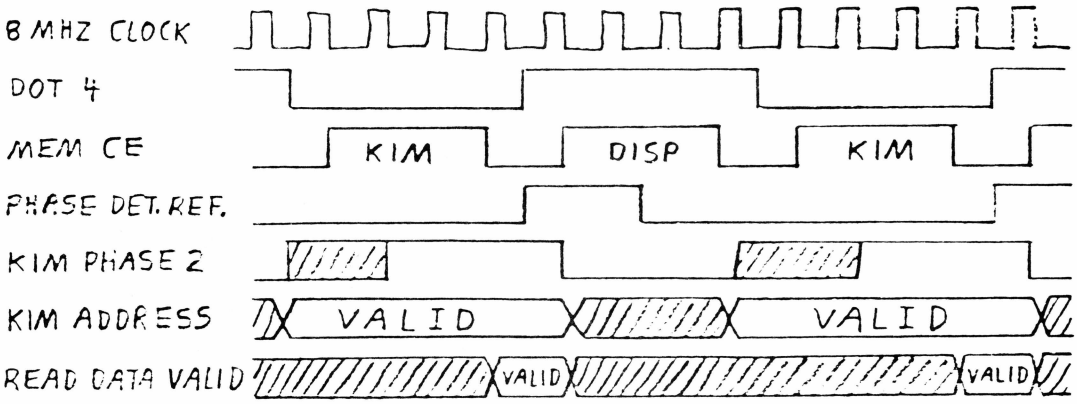
INTERFACE CIRCUITS ON K-1008 BOARD



KIM BUS INTERFACE



VIDEO OUTPUT CIRCUIT



INTERFACE TIMING

MTU K-1008 VISABLE MEMORY BLOCK DIAGRAM